DATA SHEET

BSP255

P-channel enhancement mode vertical D-MOS transistor

Product specification
Supersedes data of 1996 Jun 13
File under Discrete Semiconductors, SC07

1996 Aug 05

Philips Semiconductors

PHILIPS

P-channel enhancement mode vertical D-MOS transistor

BSP255

FEATURES

- Direct interface to C-MOS, TTL etc
- Low threshold voltage
- High speed switching
- No secondary breakdown.

APPLICATIONS

- Line current interrupter in telephone sets
- Relay, high speed and line transformer drivers.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a 4-pin plastic SOT223 SMD package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT223

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain

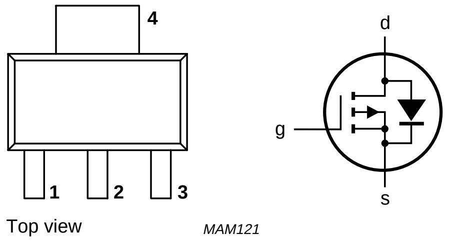


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–300	V
V_{SD}	source-drain diode forward voltage	$I_S = -0.5$ A	–	–1.8	V
V_{GS}	gate-source voltage (DC)		–	±20	V
V_{GSth}	gate-source threshold voltage	$I_D = -1$ mA; $V_{DS} = V_{GS}$	–0.8	–2	V
I_D	drain current (DC)	$T_s = 100$ °C	–	–325	mA
R_{DSon}	drain-source on-state resistance	$I_D = -160$ mA; $V_{GS} = -10$ V	–	17	Ω
P_{tot}	total power dissipation	$T_s = 100$ °C	–	4	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–300	V
V_{GS}	gate-source voltage (DC)		–	±20	V
I_D	drain current (DC)	T_s = 100 °C; note 1	–	–325	mA
I_{DM}	peak drain current	note 2	–	–1.3	A
P_{tot}	total power dissipation	T_s = 100 °C	–	4	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–65	+150	°C
Source-drain diode					
I_S	source current (DC)	T_s = 100 °C	–	–0.5	A
I_{SM}	peak pulsed source current	note 2	–	–2	A

Notes

1. T_s is the temperature at the soldering point of the drain lead.
2. Pulse width and duty cycle limited by maximum junction temperature.

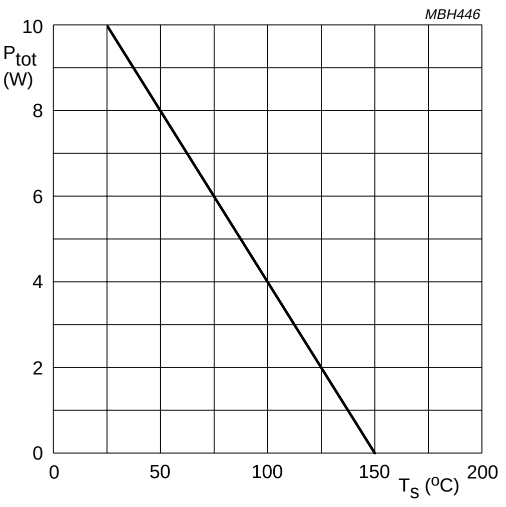
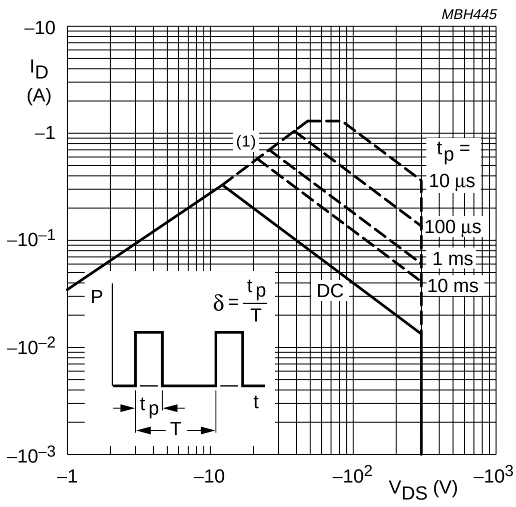


Fig.2 Power derating curve.



δ = 0.01; T_S = 100 °C.

(1) R_{DSon} limitation.

Fig.3 DC SOAR.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	12	K/W

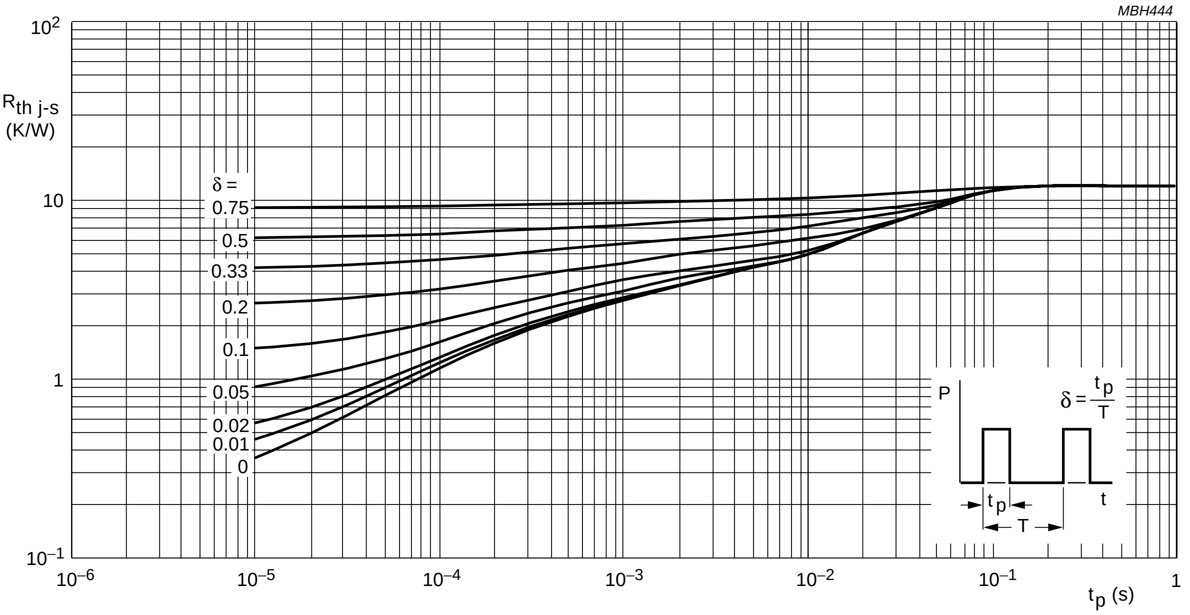
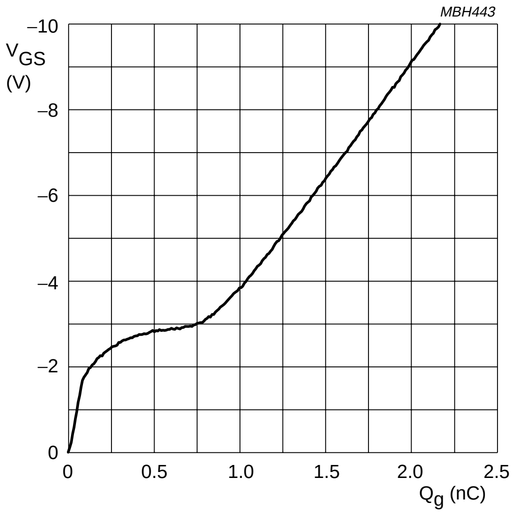


Fig.4 Transient thermal resistance from junction to soldering point as a function of pulse time; typical values.

CHARACTERISTICS

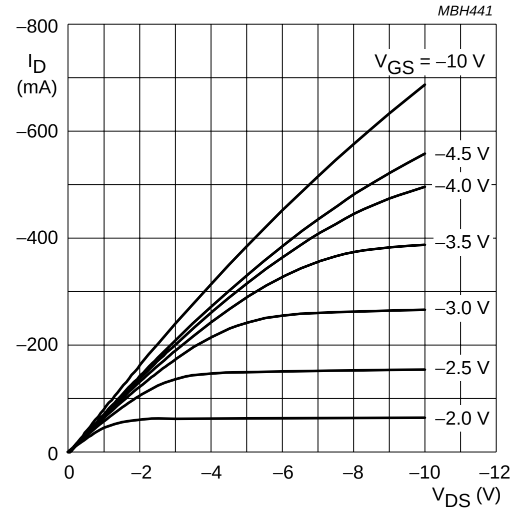
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = –10 µA	–300	–	–	V
V_{GSth}	gate-source threshold voltage	V_{GS} = V_{DS}; I_D = –1 mA	–0.8	–	–2	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = –240 V	–	–	–100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = –10 V; I_D = –160 mA	–	–	17	Ω
		V_{GS} = –4.5 V; I_D = –80 mA	–	–	20	Ω
		V_{GS} = –2.8 V; I_D = –50 mA	–	–	25	Ω
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = –50 V; f = 1 MHz	–	45	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = –50 V; f = 1 MHz	–	15	–	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = –50 V; f = 1 MHz	–	3	–	pF
Q_g	total gate charge	V_{GS} = –10 V; V_{DD} = –50 V; I_D = –160 mA; T_{amb} = 25 °C	–	2.3	–	nC
Q_{gs}	gate-source charge	V_{GS} = –10 V; V_{DD} = –50 V; I_D = –160 mA; T_{amb} = 25 °C	–	0.1	–	nC
Q_{gd}	gate-drain charge	V_{GS} = –10 V; V_{DD} = –50 V; I_D = –160 mA; T_{amb} = 25 °C	–	0.7	–	nC
Switching times (see Fig.11)						
$t_{d(on)}$	turn-on delay time	V_{GS} = 0 to –10 V; V_{DD} = –50 V; I_D = –160 mA; R_{gen} = 50 Ω	–	2.4	–	ns
t_r	rise time		–	1.6	–	ns
t_{on}	turn-on switching time		–	4	–	ns
$t_{d(off)}$	turn-off delay time	V_{GS} = –10 to 0 V; V_{DD} = –50 V; I_D = –160 mA; R_{gen} = 50 Ω	–	13	–	ns
t_f	fall time		–	12	–	ns
t_{off}	turn-off switching time		–	25	–	ns
Source-drain diode						
V_{SD}	source-drain forward voltage	V_{GD} = 0; I_S = –0.5 A	–	–	–1.8	V



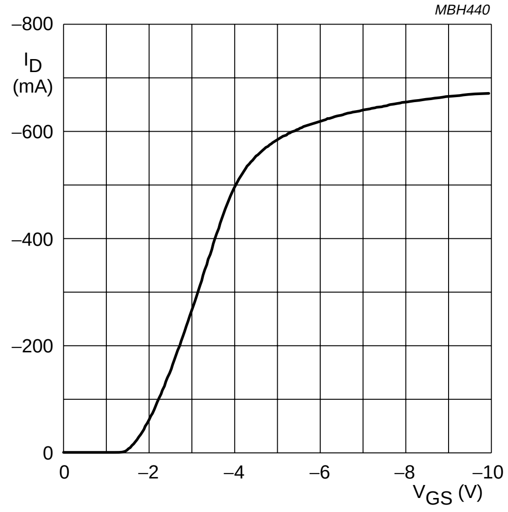
V_{DD} = −50 V: I_D = −180 mA.

Fig.5 Gate-source voltage as a function of total gate charge; typical values.



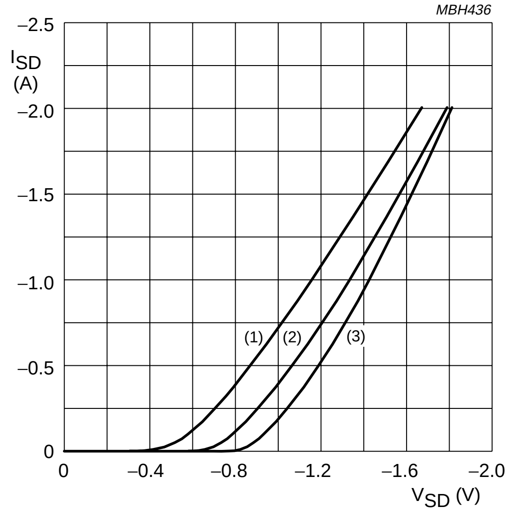
T_j = 25 °C.

Fig.6 Output characteristics; typical values.



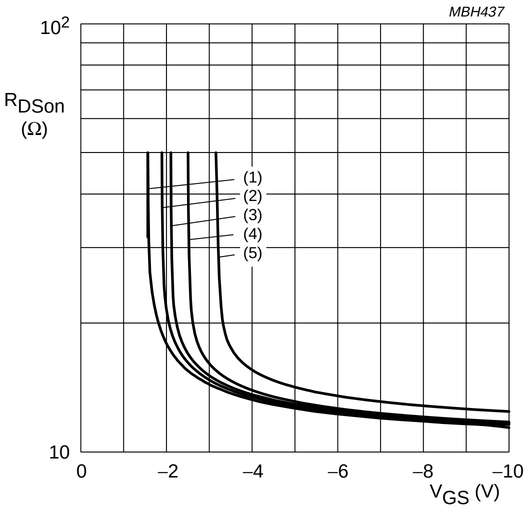
V_{DS} = −10 V; T_j = 25 °C.

Fig.7 Transfer characteristics; typical values.



V_{GD} = 0.
(1) T_j = 150 °C.
(2) T_j = 25 °C.
(3) T_j = −65 °C.

Fig.8 Source-drain current as a function of source-drain diode forward voltage; typical values.



$V_{DS} \geq I_D \times R_{DSon}$; T_j = 25 °C.

(1) I_D = −10 mA.

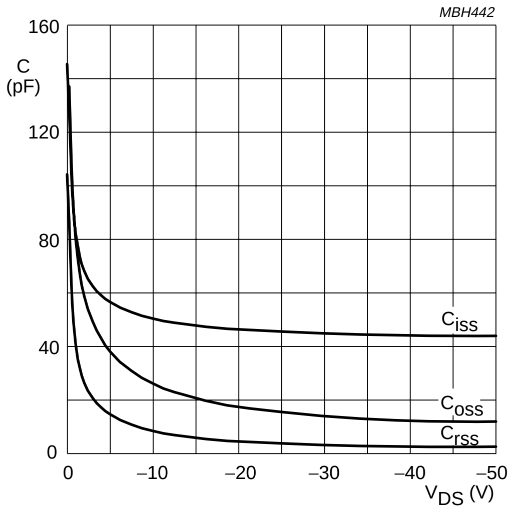
(2) I_D = −50 mA.

(3) I_D = −80 mA.

(4) I_D = −160 mA.

(5) I_D = −325 mA.

Fig.9 Drain source on-state resistance as a function of gate-source voltage; typical values.



V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.10 Capacitance as a function of drain-source voltage; typical values.

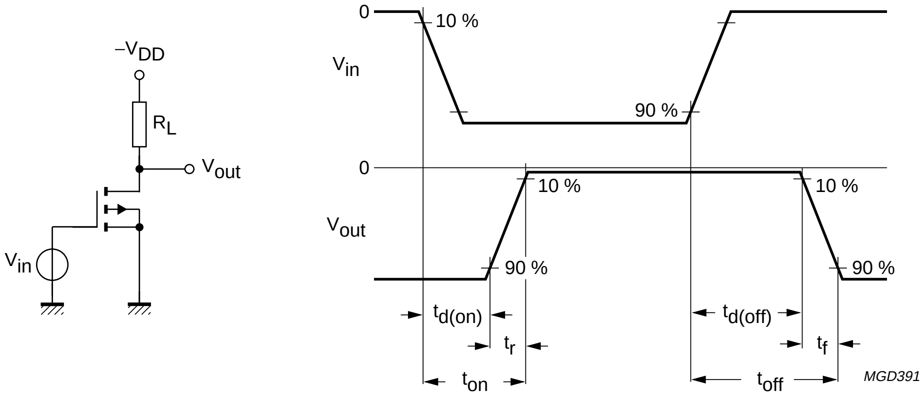
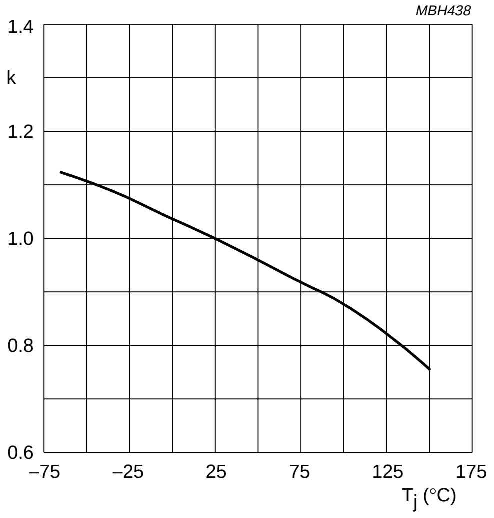


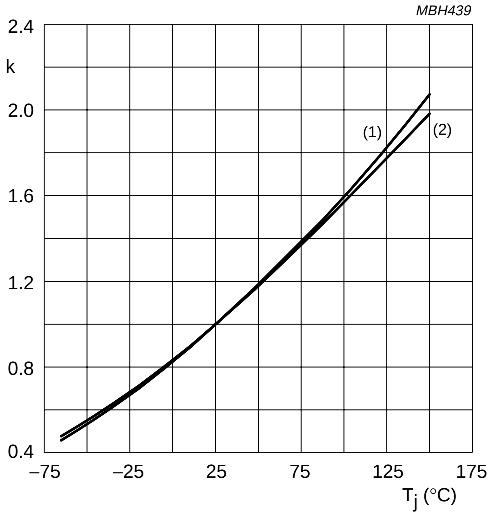
Fig.11 Switching time test circuit and input and output waveforms.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25\,°C}$$

V_{GSth} at $V_{DS} = V_{GS}$; $I_D = -1$ mA.

Fig.12 Temperature coefficient of gate-source threshold voltage as a function of junction temperature; typical values.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\,°C}$$

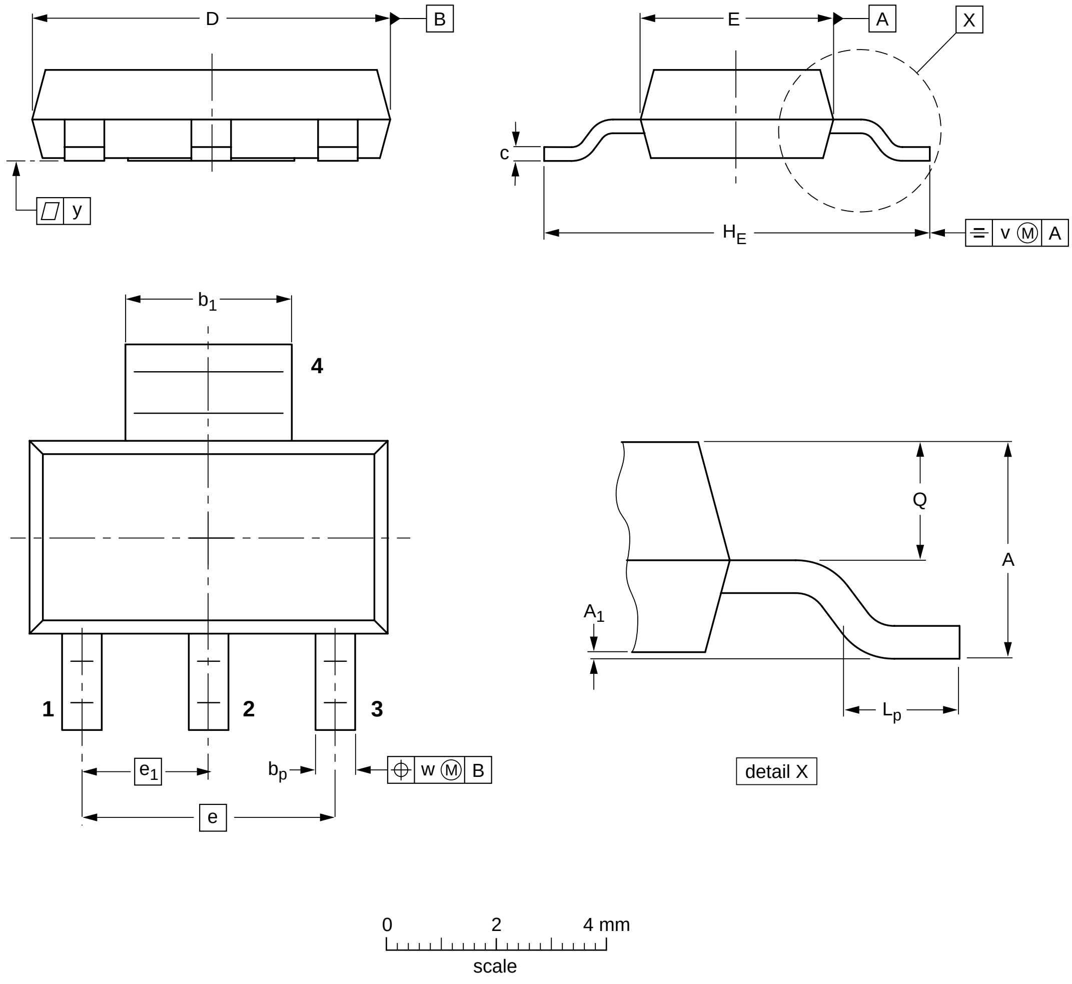
(1) $V_{GS} = -4.5$ V; $I_D = -80$ mA.

(2) $V_{GS} = -2.8$ V; $I_D = -50$ mA.

Fig.13 Temperature coefficient of drain-source on-state resistance as a function of junction temperature; typical values.

PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT223						~~96-11-11~~ 97-02-28

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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